REMARKS

In the Final Office Action dated July 15, 2005, claims 1-15 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 5,888,884 ("Wojnarowski") in view of U.S. Patent No. 6,201,631 ("Greywall"). In response, Applicant respectfully asserts that the Office Action has failed to establish a *prima facie* case of obviousness for the pending claims 1-15. In particular, the cited references of Wojnarowski and Greywall when combined do not teach or suggest all of the limitations of either claim 1 or 10, as explained below. Furthermore, there is no valid suggestion or motivation to combine the teachings of Wojnarowski and Greywall to derive the claimed invention. In view of the following remarks, Applicant respectfully requests the allowance of the pending claims 1-15.

I. Patentability of Independent Claims 1 and 10

The Office Action has rejected the independent claims 1 and 10 under 35 U.S.C. §103(a) as allegedly being unpatentable over Wojnarowski in view of Greywall. To establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), the following three basic criteria must be met, as set forth in MPEP §2143:

> "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations."

However, the cited references of Wojnarowski and Greywall when combined do NOT teach or suggest all of the limitations of either claim 1 or 10. Furthermore, there is no valid suggestion or motivation to combine the teachings of Wojnarowski and Greywall to derive the claimed invention.

A. Cited references of Wojnarowski and Greywall when combined do not teach or suggest all of the limitations of claim 1

The independent claim 1 recites in part "*electrically isolated electrodes arrayed along said layer of insulating material on said side surface*." The Office Action alleges on page 3 that Wojnarowski discloses "a plurality of electrically isolated and patterned electrodes/channels arrayed along the continuous layer of the insulating material on the side surfaces including each left and right side surface (see one of the plurality of 62/64, shown as being connected with respective one of the plurality of interconnects/pads 40 on each side surface in Fig. 8; Col. 6, lines 37-43; Col. 7, lines 49-65; also see Col. 7, lines 63-65)." Applicant respectfully disagrees.

In Fig. 8 of Wojnarowski, "hole" metallizations 62 that are connected to bottom pads 64 are shown. Each hole metallization 62 is on a particular layer of insulating material 54. The layers of insulating material 54 are shown and identified in Figs. 3-5 and 7, but not identified in Figs. 6 and 8. Each of these metallizations 62 is not on the same layer of insulating material, but rather on a different layer of insulating material. Consequently, Wojnarowski does NOT disclose "*electrically isolated electrodes arrayed along said layer of insulating material on said side surface*," as recited in claim 1.

As illustrated in Figs. 1-7 and described in the specification of Wojnarowski, each hole metallization 62 on a particular layer of insulating material 54 is formed in the following manner. First, holes 50 are formed through a wafer 30 (See Fig. 2; column 6, lines 64-65). Next, an insulating coating 54 is formed on all exposed surfaces of the wafer 30, including the top surface 32, the bottom surface 34 and surfaces within the holes 50 (See Fig. 3; column 7, lines 16-18). Opening 56 are then formed in the insulating coating on the top surface 32 to provide access to top interconnection pads 40 (See Fig. 4; column 7, lines 29-31). Next, the wafer 30 is cleaned, backsputtered and metallized on both sides, forming metallization 60 (See Fig. 5; column 7, lines 37-41). Excess metal are then removed using patterned resist, leaving patterned metal 62 (See Fig. 6; column 7, lines 46-53). Next, the wafer 30 is sawed using a dicing saw such that each metallized hole 50 is divided in two, resulting in a half-barrel appearance (See Fig. 7; column 7, lines 54-65). As a result,

for each divided "half-barrel" hole 52, one metallization 62 on a single layer of insulating material 54 is formed. Thus, Wojnarowski discloses metallizations 62 on different layers of insulating material 54 such that each metallization is on a particular layer of insulating material. Consequently, Wojnarowski does NOT disclose "*electrically isolated electrodes arrayed along said layer of insulating material on said side surface*," as recited in claim 1.

Furthermore, the different layers of insulating material 54 of Wojnarowski are not on a side surface of a separated wafer segment 70, but within channels defined by the divided "half-barrel" holes 52. When the wafer 30 is separated using a dicing saw, the side surfaces of the resulting wafer segments, such as the wafer segment 70, are the exposed surfaces between the channels. Since the layers of insulating material 54 are within these channels, the layers of insulating material are not on a side surface, as recited in claim 1. Thus, Wojnarowski does NOT disclose "*electrically isolated electrodes arrayed along said layer of insulating material on said side surface*," as recited in claim 1.

Since Wojnarowski does not disclose all of the limitations of claim 1, the cited references of Wojnarowski and Greywall when combined do NOT teach or suggest all of the limitations of claim 1. Consequently, claim 1 is not obvious in view of the cited references of Wojnarowski and Greywall.

B. There is no valid suggestion or motivation to combine the teachings of Wojnarowski and Greywall

In responding to Applicant's response to previous Office Action, the Office Action states that "Greywall teaches using the DRIE process to etch conventional electrode/conductive material including polysilicon where an etchant has etch selectivity with respect to oxide/insulating material (Fig. 4 and 5; Col. 5, lines 30-65; Col. 6, lines 35-45)" and that "[s]uch conductive structure and etch process provides an improved metal removal/etch and profile, reduced undercut and improved HDI reliability." However, the cited teaching of Greywall with respect to DRIE has nothing to do with electrodes, let alone electrodes on an insulating material on a side

surface of a semiconductor core, as recited in claim 1. Thus, there is no valid suggestion or motivation to combine the teachings of Wojnarowski and Greywall.

The cited passage of Greywall in column 5, lines 30-65, describes that DRIE can be used to form **cavities 9 in the bottom silicon layer 50** of a silicon-oxide-silicon substrate. However, the cited passage of Greywall in column 6, lines 35-45, which describes electrodes and interconnects, has nothing to do with DRIE. Consequently, the two cited passages of Greywall are not related with respect to DRIE. Thus, Greywall only discloses using DRIE to form cavities 9 in the bottom silicon layer 50, not electrodes on a side surface, as recited in claim 1

Since Greywall discloses using DRIE to form only cavities in a bottom silicon layer of a silicon-oxide-silicon substrate, Applicant respectfully asserts that there is no valid suggestion or motivation to combine the teachings of Greywall and Wojnarowski to derive the claimed invention. The only "motivation" for combining the teachings of Greywall and Wojnarowski is the rationale set forth by the Examiner, which is not supported by the cited references. Therefore, Applicant respectfully asserts that claim 1 is not obvious in view of the cited references of Wojnarowski and Greywall.

C. Independent claim 10

The independent claim 10 recites limitations that are similar to those of the independent claim 1. Therefore, the above remarks with respect to the independent claim 1 are also applicable to the independent claim 10. As such, Applicant respectfully asserts that the independent claim 10 is also not obvious in view of the cited references of Wojnarowski and Greywall.

II. Patentability of Dependent Claim 2-9 and 11-15

Each of the dependent claims 2-9 and 11-15 depends on one of the independent claims 1 and 10. As such, these dependent claims include all the limitations of their respective base claims. Therefore, Applicant submits that these

dependent claims are allowable for at least the same reasons as their respective base claims.

Applicant respectfully requests reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,
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